

What is claimed is:

1. An apparatus connectable to a computer network for circuit design verification comprising:

5 a verification result collector configured to collect a verification result of a circuit;

a data conversion and registration module configured to convert the verification result to a pre-analysis indication file;

10 an analysis information collector configured to collect analysis information about a redundant non-active portion of the circuit;

an analysis information processor configured to exclude an affect of the redundant non-active portion from the verification result and make a analysis indication file;

15 an indication file storage portion configured to store the pre-analysis indication file and the analysis indication file; and

20 a data indication controller configured to output the pre-analysis indication file and the analysis indication file.

2. The apparatus of claim 1, further comprising a file combining module configured to combine the pre-analysis indication file and the analysis indication file.

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3. The apparatus of claim 1, further comprising:

a criterion data collector configured to collect a quality standard of the circuit; and

a criterion data storage portion configured to store the quality standard.

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4. The apparatus of claim 1, wherein the data indication controller further comprises a data discriminator configured to extract an item failing the quality standard from the analysis indication file.

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5. The apparatus of claim 1, further comprising a data processor configured to extract information of a common non-active portion from the pre-analysis indication file and the verification result.

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6. The apparatus of claim 1, wherein the verification result is at least one of an RTL code coverage and a fault detecting ratio.

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7. A computer implemented method for design verification comprising:

collecting a verification result of a circuit through a computer network;

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converting the verification result to a pre-analysis indication file and storing the pre-analysis indication file in an indication file storage portion;

collecting analysis information about a redundant non-active portion of the circuit through the computer network;

excluding an affect of the redundant non-active portion  
5 from the verification result and making an analysis indication file; and

storing the analysis indication file in the indication file storage portion.

10 8. The method of claim 7, further comprising instructing a display device to show the pre-analysis indication file and the analysis indication file.

9. The method of claim 7, further comprising combining the  
15 pre-analysis indication file and the analysis indication file.

10. The method of claim 7, further comprising extracting information of a common non-active portion from the  
20 pre-analysis indication file and the verification result.

11. The method of claim 7, wherein the verification result is at least one of an RTL code coverage and a fault detecting ratio.

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12. A computer program product for controlling a computer

system so as to verify circuit designs, the computer program product comprising:

instructions configured to collect a verification result of a circuit through a computer network;

5 instructions configured to collect analysis information about a redundant non-active portion of the circuit through the computer network;

instructions configured to exclude an affect of the redundant non-active portion from the verification result and making an analysis indication file within the computer system; and

10 instructions configured to store the analysis indication file in the indication file storage portion within the computer system.

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13. The computer program product of claim 12, further comprising instructions configured to show the pre-analysis indication file and the analysis indication file by a display device.

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14. The computer program product of claim 12, further comprising instructions configured to combine the pre-analysis indication file and the analysis indication file within the computer system.

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15. The computer program product of claim 12, further

comprising instructions configured to extract information of a common non-active portion from the pre-analysis indication file and the verification result.

5 16. The computer program product of claim 12, wherein the verification result is at least one of an RTL code coverage and a fault detecting ratio.

10 17. A computer implemented method for manufacturing an integrated circuit comprising:

sending a verification result of a circuit design to an apparatus for circuit design verification through a computer network;

15 instructing the apparatus to convert the verification result to a pre-analysis indication file and store the pre-analysis indication file in an indication file storage portion;

20 sending analysis information about a redundant non-active portion of the circuit design to the apparatus through the computer network;

instructing the apparatus to exclude an affect of the redundant non-active portion from the verification result and make an analysis indication file;

25 instructing the apparatus to store the analysis indication file in the indication file storage portion;

receiving the analysis indication file from the